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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,637	03/30/2000	Fong-Shek Lam	10559/170001/P8263	8485

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EXAMINER	
WALLACE, SCOTT A	

ART UNIT	PAPER NUMBER
2671	16

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/539,637	LAM ET AL.	
	Examiner	Art Unit	
	Scott Wallace	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 12/17/03 have been fully considered but they are not persuasive. The applicant argues "Murphy reserves the active portion of the horizontal scan line for transfer of graphic data. Thus, modifying Murphy to transfer data into video line buffer based on determining when the pixel data reaches the indicator in the line buffer (i.e. during the active portion of the horizontal scan line) goes against Murphy's express teaching". However, in column 7 lines 25-30, Murphy states "After the next scan line has begun, the next burst of 128 pixels (1024 bits) is transferred once the graphic FIFO is less than half full". This is the motivation for using the indicator of Kansal. To make sure the video line buffer always has enough data to display during the horizontal blanking period.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al., U.S. Patent No. 6,172,669 in view of Kansal et al., U.S. Patent No. 5,657,055.

3. As per claims 1 and 22, Murphy et al discloses a method comprising: a line buffer to store up to a full line of video overlay data (column 4 lines 47-51 and column 5 lines 35-43); reading pixel data for a current video line from the line buffer (column 5 lines 35-47 and column 6 lines 1-10). However, Murphy et al does not specifically disclose an indicator and determining when the data reaches the indicator and loading data for the next video line into the line buffer based on the determining when the pixel data reaches the indicator. This is disclosed in Kansal et al in column 1 lines 49-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an indicator (water

mark) as in Kansal et al with the system of Murphy et al because this takes advantage of idle system memory bus and allows other devices to gave earlier access to the system.

4. As per claim 2, Murphy et al discloses wherein setting the indicator in the line buffer comprises setting the indicator at approximately a middle of the line buffer (column 6 lines 22-31, there is some indication when the FIFO is half full, therefore this is the same as setting an indicator at the middle mark because when the data reaches this mark there is only half of it left), and wherein loading data for the next video line into the line buffer comprises loading a first half of the data for the next video line when the pixel data being read reaches the indicator in the line buffer (column 6 lines 1-31), and further comprises loading a second half of the data for the next video line when the pixel data being read reaches the end of the line buffer (column 6 lines 1-31).

5. As per claim 3, Murphy et al discloses wherein loading data for the next video line comprises: loading a first portion of the data for the next video line when the pixel data reaches the indicator (column 6 lines 22-31, there is some indication when the FIFO is half full, therefore this is the same as setting an indicator at the middle mark because when the data reaches this mark there is only half of it left); and loading a second portion of the data for the next video line when the pixel data reaches the end of the line buffer (column 6 lines 1-31).

6. As per claim 4, Murphy et al discloses further comprising processing the current video line data for the display (column 4 lines 47-51 and column 5 lines 35-47).

7. As per claim 5, Murphy et al discloses displaying the processed video line data (column 6 lines 35-47).

8. As per claim 6, Murphy et al discloses creating a video overlay from the processed video line data (fig 1 and column 4 lines 47-51).

9. As per claim 7, Murphy et al discloses positioning the pixel data on an active display to create a video overlay (fig 1 and column 4 lines 47-51).

10. As claim 8, Murphy et al discloses a method of processing video overlay data comprising: reading video overlay data for a current video line from a line buffer, the line buffer to store up to a full line of the video overlay data. However, Murphy et al does not specifically disclose detecting the position in the line

buffer the video overlay data is located and loading the next line of video depending on this detection. This is disclosed in Kansal et al in column 1 lines 49-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an detection step (water mark) as in Kansal et al with the system of Murphy et al because this takes advantage of idle system memory bus and allows other devices to gave earlier access to the system.

11. As per claim 9, Kansal et al discloses setting the predetermined positioned at a position before all the current line of video overlay data is read (column 1 lines 49-65).

12. As per claim 10, Murphy et al discloses wherein the predetermined position is at approximately a midpoint of the line buffer (column 6 lines 22-31, there is some predetermined position when the FIFO is half full, therefore this is the same as setting a predetermined position at the middle mark because when the data reaches this mark there is only half of it left), and wherein loading data for the next video line into the line buffer comprises loading a first half of the data for the next video line after the video data for the current video line has been read from the predetermined position (column 6 lines 1-31), and further comprises loading a second half of the data for the next video line after the video data for the current video line has been read from the end of the line buffer (column 6 lines 1-31).

13. As per claim 11, Murphy et al discloses wherein loading data for the next video line comprises: loading a first portion of the data for the next video line into the line buffer when the video data from the predetermined position has been read (column 6 lines 22-31, there is some indication when the FIFO is half full, therefore this is the same as setting an indicator at the middle mark because when the data reaches this mark there is only half of it left); and loading a second portion of the data for the next video line into the line buffer when the video data from the end of the line buffer has been read (column 6 lines 1-31).

14. As per claim 12, Murphy et al discloses further comprising processing the current video line data for the display (column 4 lines 47-51 and column 5 lines 35-47).

15. As per claim 13, Murphy et al discloses displaying the processed video line data (column 6 lines 35-47).

16. As per claim 14, Murphy et al discloses a overlay display processor (fig 1) comprising: a line buffer to store up to a full line of video overlay data (column 5 lines 35-47), the line buffer having a plurality of memory locations (column 5 lines 35-67), the line buffer adapted to provide data to a display (column 5 lines 35-67). Murphy et al does not specifically disclose an indicator and wherein the line buffer begins to read data for a next video line when the line buffer provides data from the indicator. This is disclosed in Kansal et al in column 1 lines 49-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an indicator (water mark) as in Kansal et al with the system of Murphy et al because this takes advantage of idle system memory bus and allows other devices to gave earlier access to the system.

17. As per claim 15, Murphy et al discloses a graphic memory which provides the video pixel data to the line buffer (column 5 lines 35-47); and a pixel processing engine to determine whether data for a current video line has been read from the predetermined memory location in the line buffer (column 6 lines 1-31), the pixel processing engine further to subsequently load a first portion of data for the next video line into the line buffer (column 6 lines 1-31).

18. As per claim 16, Murphy et al discloses wherein the line buffer provides data to the display for a current video line (column 5 lines 35-47).

19. As per claims 17 and 23, Murphy et al discloses wherein the indicator is located at a position at approximately a midpoint of the line buffer (column 6 lines 1-31).

20. As per claim 18, Murphy et al discloses a overlay system comprising: video memory which stores video data (column 5 lines 35-47); an overlay processing engine comprising; a line buffer to store up to a full line of video overlay data (fig 1 and column 4 lines 47-51 and column 5 lines 35-47), the line buffer to receive the video overlay data from the video memory (column 5 lines 35-47); video processing circuitry to prepare the video overlay data in the line buffer to be displayed (column 5 lines 35-47); and a display to receive the processed data from the overlay processing engine (fig 1), wherein the line buffer is to read data for a next video data line when the line buffer provides a predetermined amount of data to the display for a current video data line (column 6 lines 1-31). Murphy et al does not specifically disclose an indicator. This is disclosed in Kansal et al in column 1 lines 49-65. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to use an indicator (water mark) as in Kansal et al with the system of Murphy et al because this takes advantage of idle system memory bus and allows other devices to gave earlier access to the system.

21. As per claim 19, Murphy et al discloses wherein the predetermined amount of data is approximately half the data comprising the current video data line (column 6 lines 1-31).

22. As per claim 20, Murphy et al discloses wherein the overlay processing engine provides data to the display to create a video overlay (fig 1 and column 4 lines 47-51).

23. As per claim 21, Murphy et al discloses wherein the video processing circuitry includes pixel color conversion and adjustment (column 5 lines 35-55).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Scott Wallace** whose telephone number is **703-605-5163**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached at 703-305-9798.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600